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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/805,742	03/13/2001	Brian W. Huber	500894.01	3868

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EXAMINER	
BURD, KEVIN MICHAEL	
ART UNIT	**PAPER NUMBER**
2631	

DATE MAILED: 12/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/805,742	HUBER, BRIAN W.	
	Examiner	Art Unit	
	Kevin M. Burd	2631	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a).. In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-56* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4,7-9,11-13,15-22,25-27,29-35,38-40,42-46,48-54 and 56* is/are rejected.

7)☒ Claim(s) *5,6,10,14,23,24,28,36,37,41,47 and 55* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *13 November 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Drawings

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the at least one output terminal must be shown or the feature canceled from the claims. The other terminals appear to be shown (the first and second input terminals and the input/output terminal) but the output terminal does not appear to be shown. No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 1-15 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The specifications do not appear to disclose the at least one output terminal as stated in the claims. The other terminals are described in the specification and drawings but the description of the output terminal does not appear in the specifications. Clarification or correction is required.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1-4, 7-9, 11-13, 15, 42-46, 48-54 and 56 are rejected under 35 U.S.C. 103(a) as being unpatentable over the instant application's disclosed prior art (specifically figure 1) in view of Urabe et al (US 5,369,409).

Regarding claims 1, 9, 11, 42, 48, 49 and 56, figure 1 of the instant application discloses a digital differential input receiver circuit comprising first and second input terminals (36a and 38a) and an input/output terminal 44a. A reference voltage source 40 is connected to the second input terminal. The differential input receiver does not disclose an isolation circuit coupled to the circuit to isolate a terminal from the reference voltage in response to an activation signal and an output signal detector for generating the activation signal.

Urabe discloses a circuit that provides near perfect isolation between the input terminal and the output terminal (column 9, lines 20-23). The output signal is used as an input to the timing control signal 54 on figure 1 and renders the switching transistors Q2 and Q1 active (column 9, lines 4-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the isolation capability taught in Urabe into the prior art of the instant application to prevent signals from the input terminal from leaking to the output terminal when no signal is to be output. The field effect transistors S1 and S2 in figure 2 operate as the logic gate.

Regarding claims 2, 3, 12, 13, 43, 44, 51 and 52, the isolation circuit is coupled between the input and output terminals.

Regarding claim 4, the isolation circuit is coupled between the input terminal and the output terminal and is operable as stated above.

Regarding claims 7, 8, 15, 45, 46, 50, 53 and 54, the differential input receiver includes a pair of differential transistors coupled to each other and comprising a bias circuit as shown in figure 1 of the instant application.

4. Claims 16-22, 25-27, 29-35 and 38-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over the instant application's disclosed prior art (specifically figure 1) in view of Urabe et al (US 5,369,409) further in view of Estakhri (US 6,374,337).

Regarding claim 16, 19, 22 and 27, Estakhri discloses a memory device shown in figures 1 and 2. The memory device comprises a memory array 10, an address decoder 12, a command register 24, an input buffer 20 and an output buffer 34. Additional information is provided in column 3, lines 23-53. This column provides information concerning reading and writing to the memory and the control signals used. Estakhri does not disclose specifics concerning the data input buffer.

Figure 1 of the instant application discloses a plurality of digital differential input receiver circuits each comprising first and second input terminals (36a and 38a) and an input/output terminal 44a. A reference voltage source 40 is connected to the second input terminal. It would have been obvious for on of ordinary skill in the art at the time of the invention to incorporate the input receivers of the instant application into the input buffer of Estakhri to allow the data buffer to receive and correctly store all the information input to the buffer.

The combination of Estakhri and the instant application's disclosed prior art does not disclose isolation circuits coupled to each of the input receivers to isolate a terminal from the reference voltage in response to an activation signal and an output signal detector for generating the activation signal in each of the input receivers.

Urabe discloses a circuit that provides near perfect isolation between the input terminal and the output terminal (column 9, lines 20-23). The output signal is used as an

input to the timing control signal 54 on figure 1 and renders the switching transistors Q2 and Q1 active (column 9, lines 4-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the isolation capability taught in Urabe into the combination of Estakhri and the prior art of the instant application to prevent signals from the input terminal from leaking to the output terminal when no signal is to be output. The field effect transistors S1 and S2 in figure 2 operate as the logic gate.

Regarding claims 17 and 18, figure 1 of the instant application discloses the output drivers 44

Regarding claims 20 and 21, the isolation circuit is coupled between the input and output terminals.

Regarding claims 25 and 26, the differential input receiver includes a pair of differential transistors coupled to each other and comprising a bias circuit as shown in figure 1 of the instant application.

Regarding claims 29, 32, 35 and 40, Estakhri discloses a memory device shown in figures 1 and 2. The memory device comprises a memory array 10, an address decoder 12, a command register 24, an input buffer 20 and an output buffer 34. Additional information is provided in column 3, lines 23-53. This column provides information concerning reading and writing to the memory and the control signals used. Estakhri discloses a host computer in 101. A computer inherently comprises a number of components including a processor, system controller, buses input device, output

device and a storage device such as a hard drive. All of these components will be found in all computers. Estakhri does not disclose specifics concerning the data input buffer.

Figure 1 of the instant application discloses a plurality of digital differential input receiver circuits each comprising first and second input terminals (36a and 38a) and an input/output terminal 44a. A reference voltage source 40 is connected to the second input terminal. It would have been obvious for on of ordinary skill in the art at the time of the invention to incorporate the input receivers of the instant application into the input buffer of Estakhri to allow the data buffer to receive and correctly store all the information input to the buffer.

The combination of Estakhri and the instant application's disclosed prior art does not disclose isolation circuits coupled to each of the input receivers to isolate a terminal from the reference voltage in response to an activation signal and an output signal detector for generating the activation signal in each of the input receivers.

Urabe discloses a circuit that provides near perfect isolation between the input terminal and the output terminal (column 9, lines 20-23). The output signal is used as an input to the timing control signal 54 on figure 1 and renders the switching transistors Q2 and Q1 active (column 9, lines 4-9). It would have been obvious for one of ordinary skill in the art at the time of the invention to incorporate the isolation capability taught in Urabe into the combination of Estakhri and the prior art of the instant application to prevent signals from the input terminal from leaking to the output terminal when no signal is to be output. The field effect transistors S1 and S2 in figure 2 operate as the logic gate.

Regarding claims 30 and 31, figure 1 of the instant application discloses the output drivers 44

Regarding claims 33 and 34, the isolation circuit is coupled between the input and output terminals.

Regarding claims 38 and 39, the differential input receiver includes a pair of differential transistors coupled to each other and comprising a bias circuit as shown in figure 1 of the instant application.

Allowable Subject Matter

5. Claims 5, 6, 10, 14, 23, 24, 28, 36, 37, 41, 47 and 55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chen et al (US 6,040,731) discloses an isolation circuit coupled between the input circuit and the output circuit (figure 3).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kevin M. Burd whose telephone number is (571) 272-3008. The examiner can normally be reached on Monday - Thursday 9 am - 5 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mohammad Ghayour can be reached on (571) 272-3021. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Kevin M. Burd
12/1/2004

KEVIN BURD
PRIMARY EXAMINER